REMARKS

This application has been reviewed in light of the Office Action dated May 16, 2005.

Claims 21-26 are now presented for examination. Claim 21, the only independent claim, has been amended to more particularly point out and distinctly claim the subject matter regarded as the invention. Favorable review is respectfully requested.

Claims 21-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Pogge (U.S. Pat. No. 6,110,806) in view of Dordi (U.S. Pat. No. 5,835,355). The applicants respectfully submit that independent claim 21, as amended, is patentable over the art cited by the Examiner, for the following reasons.

The present invention, as defined in claim 21, is directed to an integrated structure which includes a first layer having a first set of conductors, a semiconductor device, a second layer having a second set of conductors, a plurality of connectors, and a support structure. The Examiner states that several features of the invention recited in the claim are found in the Pogge reference. The applicants wish to respectfully point out that the Examiner has not correctly characterized the structure disclosed in the Pogge reference. In the marked-up copy of Pogge Figure 10 provided by the Examiner, thin films with metal lines (Pogge, col. 4, lines 62-65) are labeled as corresponding to the first, second and third layers of the present invention. None of these films (or a combination of such films) meets the requirements of the first layer as recited in claim 21. The underside of the films 82 has small areas of metal at the interface with glass substrate 85 (see Pogge, Figure 9), but does not have bonding pads as in the present invention. The glass substrate 85 in Pogge is a temporary holding plate (see Pogge, col. 5, lines 23-28), does not offer any electrical connections, is not part of the final structure of Pogge, and thus cannot be viewed as a motherboard.

In addition, Pogge does not offer any teaching or suggestion regarding spacing between the areas of metal in films 82; these areas are shown without any particular spacing, and cannot be viewed as bonding pads having a spacing as in the present invention.

It is also a feature of the present invention that a support structure surrounds the semiconductor device, and is attached to the upper surface of the first layer and is in contact therewith. No such structure is disclosed or suggested in the Pogge reference. The Examiner has labeled two of the chips 30 in Pogge as "support structure." However, there is no suggestion in Pogge that any of the chips surround other chips. Furthermore, the Examiner suggests that Pogge meets the requirements of the claim by characterizing the uppermost thin film 82 as the second layer. Claim 21 has been amended to explicitly recite that the support structure is in contact with the first layer; that is, a layer having conductors connecting to bonding pads. In the embodiment of the invention shown in Figure 4B of the specification, stiffener 41 (including adhesive layer 42) surrounds chip 31 and is in contact with layer 26/28 (wiring layer 26 with adhesive layer 28). In Figure 10 of Pogge, by contrast, the chips 30 are in contact with and connected to a plurality of thin films 82, with no connection to bonding pads on the underside of those films.

Pogge therefore does not disclose or suggest a first layer, a second layer, or a support structure as recited in claim 21. The present invention therefore would not have been obvious from the Pogge reference.

The Examiner states that Pogge fails to disclose a plurality of connector structures disposed on the lower surface of the first layer, and points to Dordi as supplying this feature. The applicants wish to point out that "a plurality of connector structures disposed on the lower surface of the first layer" is not recited in the claims; the Examiner's statement therefore is not understood. Dordi appears to disclose a ball grid array package in which a chip 12 connects to a tape 16; the tape is typically made of a dielectric material sandwiched between two layers of copper (Dordi, col. 4, lines 49-52). The tape 16 of Dordi does not correspond to the first layer of the present invention, since the tape does not have bonding pads disposed on a lower surface thereof. Dordi therefore does not disclose or suggest a first layer as in the present invention.

Dordi also does not disclose or suggest a second layer as in the present invention, but merely refers to interconnection points on chip 12. Furthermore, the chip connections 14 of Dordi are not spaced with respect to each other with a spacing distance less than the spacing distance corresponding to the motherboard connections, as in the present invention. Indeed,

Figures 1 and 5 of Dordi show the chip connections having a larger spacing than the connections between the tape and the board.

A combination of Pogge and Dordi would at best yield a structure where chips are brought into alignment using polyimide alignment structures, and then connected to a board using a tape ball grid array. Such a structure would not have a first layer or second layer, have a support structure in contact with the first layer, as recited in independent claim 21.

Accordingly, the present invention would not have been obvious from either of the two cited references, or from a combination thereof.

The other claims in this application are each dependent from the independent claim discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, the applicants respectfully request favorable reconsideration and early passage to issue of the present application.

The applicants' undersigned attorney may be reached by telephone at (845) 894-3667. All correspondence should continue to be directed to the below listed address.

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